A SYSTEM FOR CLOCK DUTY CYCLE STABILIZATION

ABSTRACT OF THE DISCLOSURE

A clock signal duty cycle stabilization system. The system includes a clock signal duty cycle stabilization circuit having an edge detection circuit and a latch circuit. The edge detection circuit is configured to receive an external clock signal and generate an output therefrom. The latch circuit is coupled to receive the output from the edge detection circuit. The latch circuit is configured to produce a rising edge of an internal clock signal and a falling edge of the internal clock signal in accordance with the output of the edge detection circuit.